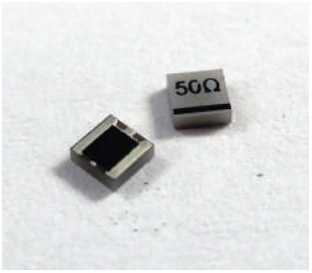
Broadband DC - 44GHz Testing of Chip Termination

BAN-TV0808ZZ-50R0JN-2S

Barry Application Note

Purpose & Scope:



The intent of this experiment was to measure the return loss of a Barry chip termination, part number TS0808CT-50R0JN-2S, to the upper frequency limit of the Vector Network Analyzer (VNA) used for the test. The range of the VNA used is 40MHz to 65GHz. The following equipment was used:

- TS0808CT-50R0JN-2S Chip Terminations Mounted on Rogers 4003
- DC–65GHz Anritsu Vector Network Analyzer – Model 37397A
- Hasco 2.92mm 18” Cables – Model HLL150-29P-29J-18
- Southwest Microwave 2.92mm Launchers – Model SWI-1092-02A-5

Assembled fixture can be seen in Figure 1.

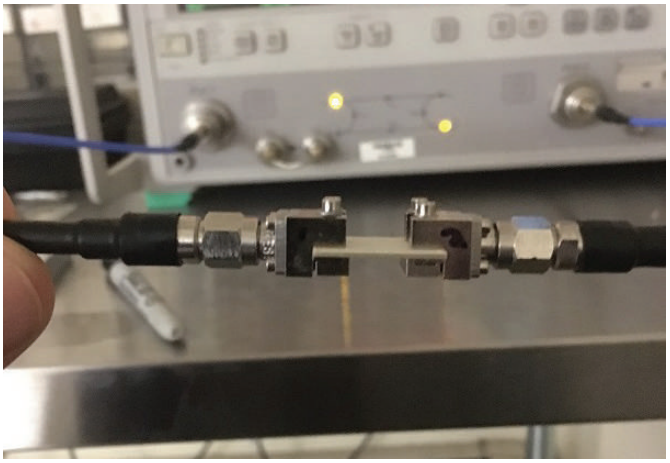


Figure 1

Part Design

The TS0808CT-50R0JN-2S is a 50 ohm impedance, 0.08” x 0.08” sized thick film on 0.025” AlN chip termination. See Figure 2.. The resistor element is constructed of glass passivated Ruthenium Oxide. The device is designed for ‘face’ (film side) down mounting and features solderable terminals. See Figure 3.

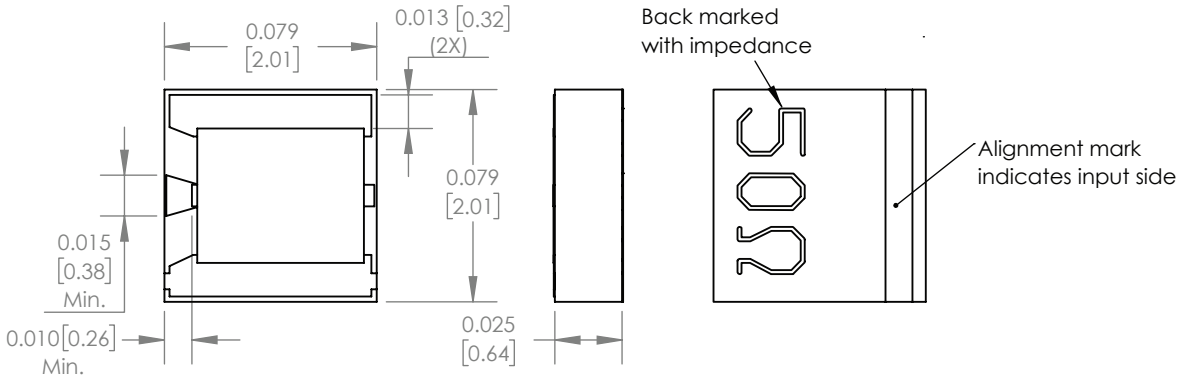


Figure 2

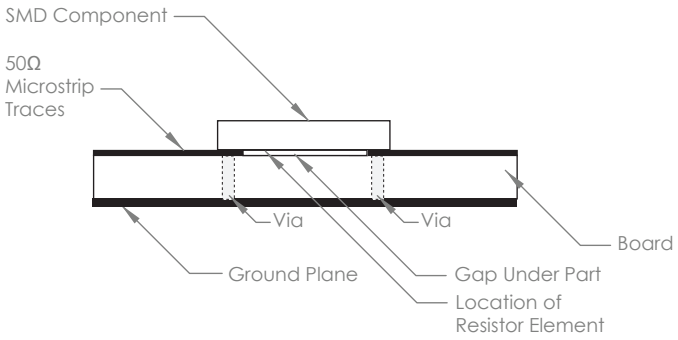


Figure 3

Calibration

Calibration is done using microstrip standards and a Line-Reflect-Line (LRL) calibration on the Anritsu VNA 37397A. The Standards are as follows and are depicted in Figure 4:

a. Through 0mm Offset
b. Through 1.25mm Offset
c. Through 10mm Offset
d. Short
e. Open
f. Load (RK0402CT-50R0JN-91 mounted on board at 0mm Offset)

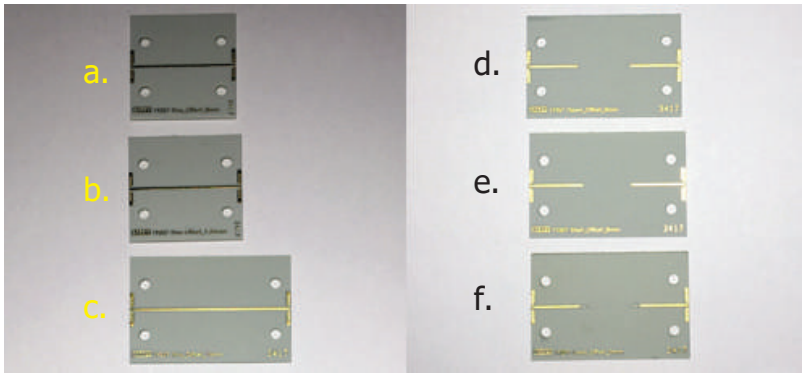


Figure 4

The AppCAD calculation for the microstrip is depicted in Figure 5 and valid frequency range of calibration for the two line offsets is calculated in Figure 6 using the methodology described Anritsu Application Note titled *'LRL/LRM Calibration'* (see separate document within this data packet)

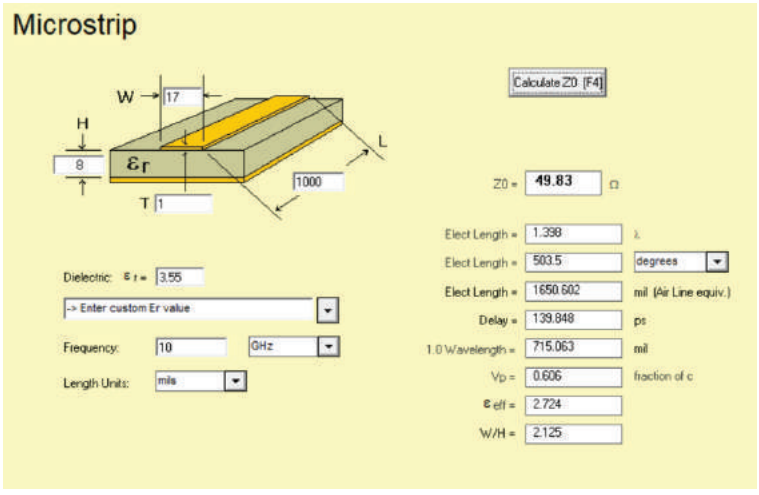


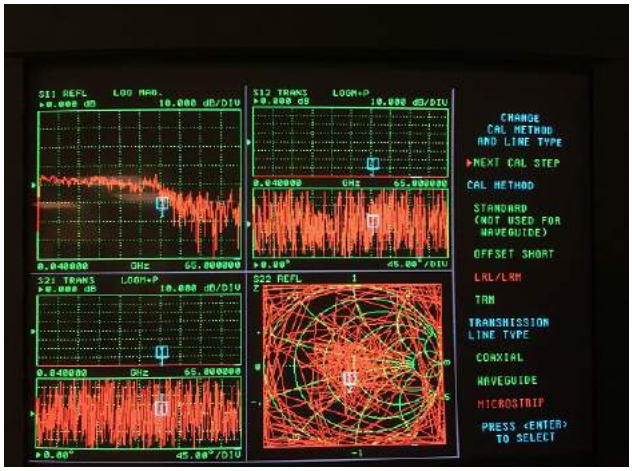
Figure 5

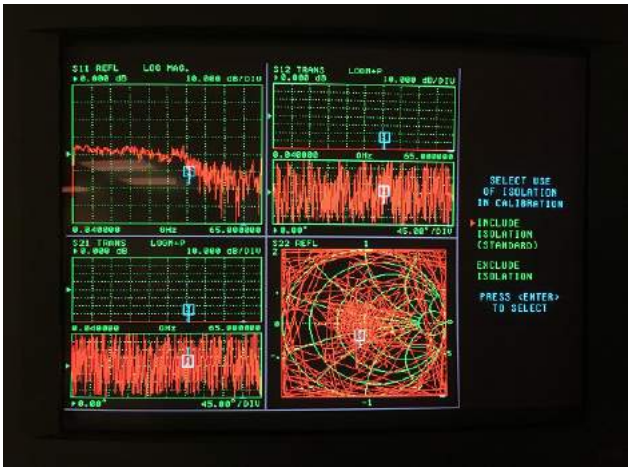
Dielectric: RO4003 er=	3.55	
Relative Permittivity	2.72	From AppC
Substrate Thickness 0.2032mm (8 mil)		
Trace Width=0.4318mm (17 mil)		
fl cutoff (degrees)	10	
fh cutoff (degrees)	160	
line offset (mm)	fl (GHz)	fh (GHz)
1.25	4.039431	64.63089
10	0.504929	8.078862

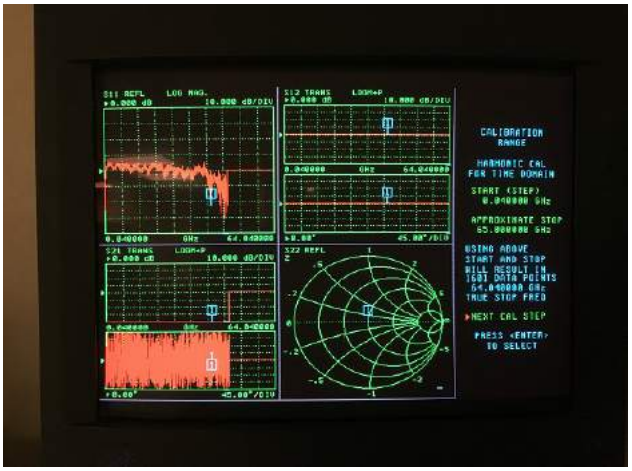
Figure 6

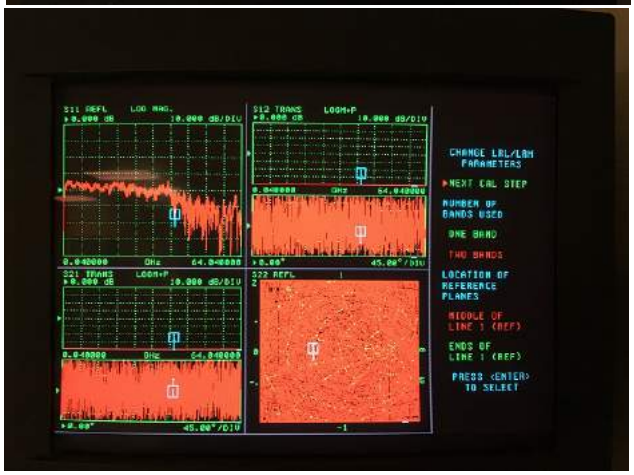
Calibration (*con't*):

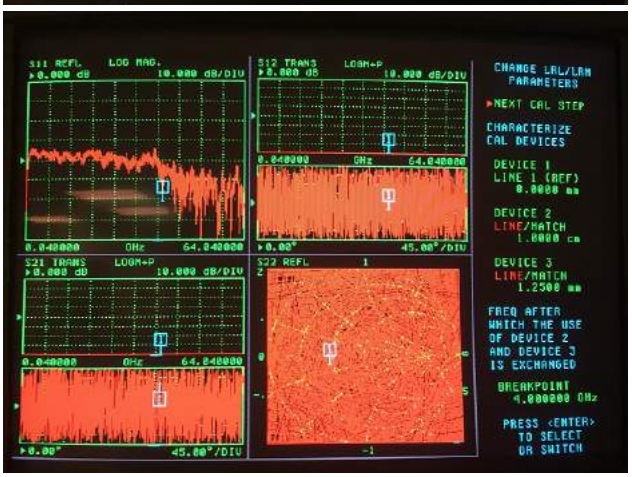
The initial approach will be to use the two offset lines to perform a calibration. This will yield questionable results for the lowest portion of the measurement range. This calibration will be used to measure the return loss of the load standard and determine an upper frequency of valid use for this standard. If the frequency is high enough, a 2 band calibration can be employed using the 1.25mm offset for the upper band and the load for ~DC to the lower limit of the 1.25mm standard. If it is not, a lowband calibration will be needed and merged to the 2 offset line calibration. The VNA calibration was configured to use the two offset lines and the open circuit standard as shown in these screen capture images:



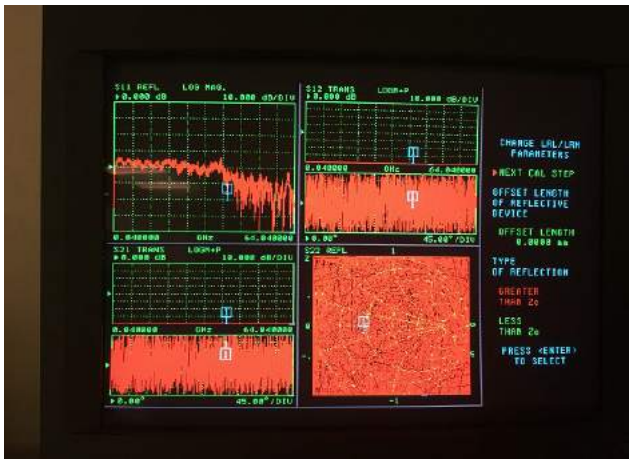


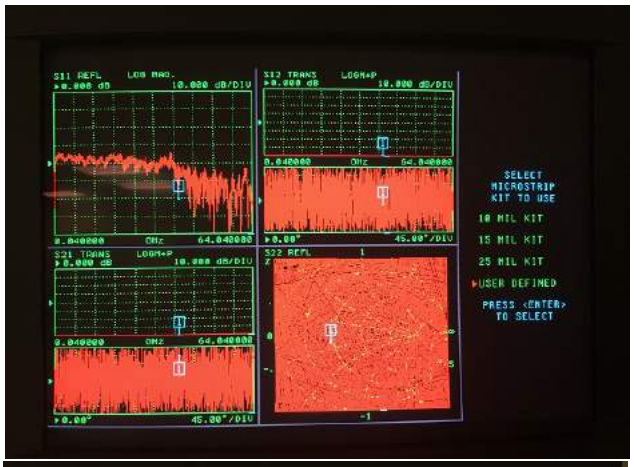


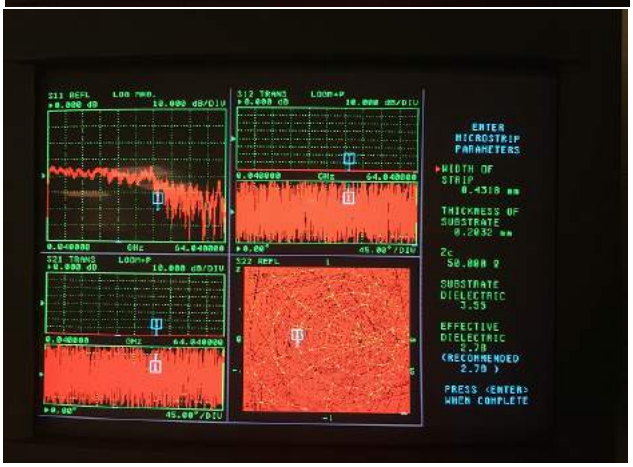




Calibration (*con't*):







Note: *The SWI-1092-02A-5 launchers are specified to 40 GHz. We will measure to 64 GHz but expect degradation in measurements above 40 GHz. Also, the same two launchers will be used to measure each standard and DUT. In addition, each one is numbered as shown in the image above and care taken to ensure that the same launcher is used at the same port of the VNA for each measurement. This will ensure that launcher to launcher differences are not adding to the measurement uncertainty.*

After performing the calibration as described above, the load standard was measured and exhibited the performance seen in Figure 7 (the two terminations were measured as a two port and therefore the data is contained within one S-parameter file including measurement of the isolation between the structures. Plotting the return loss to 10 GHz shows an abrupt transition at 4 GHz. This is likely a measurement artifact due to the transition from the calibration using the 10mm offset and the calibration using the 1.25mm offset.

Figure 8 is the same data on a Smith Chart to 40 GHz showing that the gradual degradation is due to series inductance. The loads, therefore, could be used in place of the 10mm offset if performance close to DC is of interest where the theoretical lower limit of the 10 mm offset is 500 MHz. The loads, therefore, could be used in place of the 10mm offset if performance close to DC is of interest where the theoretical lower limit of the 10 mm offset is 500 MHz.

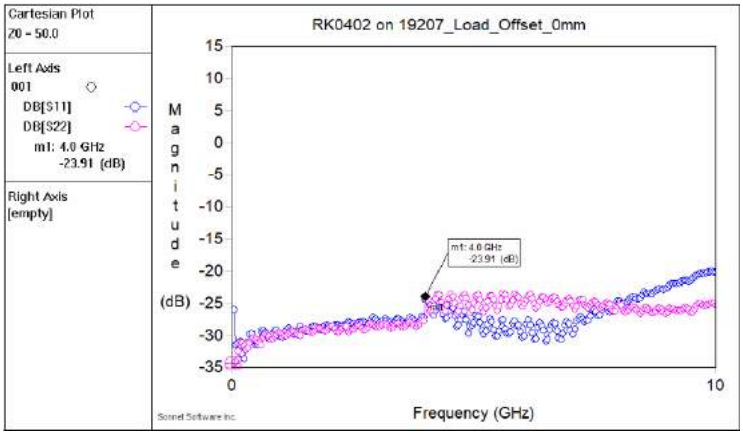


Figure 7

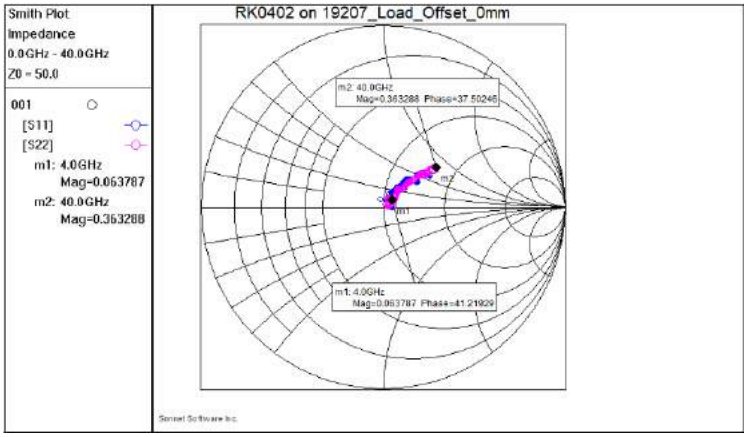


Figure 8